EFFICIENT DEVELOPMENT OF HIGHLY LINEAR MMIC POWER AMPLIFIERS

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ABSTRACT

Highly linear power amplifiers are key components of high capacity radio transmitters. This paper describes the complete procedure we established to develop a family of new MMIC power amplifiers aimed at achieving state-of-the-art performance as needed for a new M-QAM microwave radio. A cost effective approach dedicated to volume production has been addressed. The most important experimental characteristics for each of the developed MMIC PAs are also reported in order to demostrate the effectiveness of the presented procedure.

INTRODUCTION

MMIC technology is well recognized for its capability of reducing cost, size, weight and number of parts of modern microwave digital radios. Monolithics are easily integrable inside multi chip modules (MCM) and they are tuneless, therefore they are suitable for volume production and automatic testing. When dealing with high spectral efficiency modulation schemes for the radio, for example 128 or 256 QAM, improving trade-offs between linearity and power-added efficiency in power amplifiers becomes very important. The conventional approach usually consists in designing and optimising the power amplifier (PA) to yield its maximum power added efficiency, or output power at 1dB gain compression and then operating the amplifier with a sufficient output power back-off to achieve the required intermodulation level. This, however cannot be considered as a real optimization of performance. It is worth noting that power added efficiency is also extremely important in highly linear MMIC PA because it directly affects the device channel temperature and hence the reliability figure, a crucial point in modern telecommunication systems applications.

DEVELOPMENT PROCEDURE

We propose an approach for custom MMIC PA design where a trade-off between linearity and power-added efficiency is taken into consideration from the beginning of the design activity.

The development procedure we established can be summarised with the following main steps:

1. Careful choice of the active device technology and transistor unit cell topology selection. By means of experimental characterisation of test devices assembled onto the same carrier by using the same assembling process as in the final circuit application, the unit cell featuring the best trade-off of performance in the frequency range of interest among a set of different candidate structures is chosen. In this way, self-heating effects are also taken into consideration and thermal resistance can be experimentally evaluated, for a realistic MTTF figure estimation.
2. Optimum bias point identification. The maximum cell linearity is in principle obtained minimising the third order transconductance (g_{m3}), in any case taking into account the desired gain and the maximum output power for a certain bias point. The choice can be made after accurate measurements of the device's non-linear transconductance. There are many techniques

allowing the non-linear transconductance measurement as a function of V_{gs}, V_{ds} and I_d; a correct data analysis must also take into account the effect of parasitic elements (Reynoso-Hernàndez et al., (1)). In fig. 1 some transconductance values obtained from S-parameter measurements, after parasitics de-embedding, are shown.

3. Characterisation of the load dependence for both C/I3 and PAE at any fixed output power of interest by non-linear transistor load-pull measurements (Tab. 1 and Tab. 2). In many cases a compromise solution between minimum C/I3 and maximum PAE must be adopted.
4. Development of an advanced model of the active device (see, for instance, Filicori et al., (2)), able to characterise both its weakly non-linear behaviour and its linear behaviour up to the third harmonics. Before starting the design, the model should be validated by the load-pull C/I3 measured data.
5. Design and evaluation of on-chip passive elements (lumped and distributed) and off-chip passive circuits (bias circuitry and input/output chip to substrate RF interconnection) over a very broadband frequency range, starting from DC up to at least the third harmonic of the maximum operating frequency. However most important foundries generally provide accurate models for all the passive elements they produce. To further increase the accuracy in the evaluation of parasitic effects, some electromagnetic simulations of all the passive structures must be performed.
6. Determination of the required number of stages and number of unit cells for each stage. It is important to notice that the number of amplification stages may impact the overall C/I3 of the device (Maas, (3)). The number of unit cells, instead, is generally chosen taking into account the thermal dissipation efficiency.
7. MMIC design with the aid of both linear and non-linear simulations and experimental load-pull data, taking into consideration the actual environment in which the chip will be working. It's also important at this step to evaluate the design sensitivity and to estimate the yield by means of Montecarlo simulations.
8. Accurate MMIC experimental characterisation and back-end design and modelling verification.

PAxx-xx: HIGHLY LINEAR POWER AMPLIFIER FAMILY

Following the procedure described in the preceding section, a family of new MMIC power amplifiers has been designed. Their main measured electrical performance characteristics as currently available are reported in Tab. 3. Careful selection of the most suitable foundry technology process was the first very important step that was undertaken, cost effectiveness for volume production being the primary driver for the design development. Several transistor basic cells with different topologies and gatewidths were then designed and characterised by means of "directly on-chip" measurements. The selected basic active device was then experimentally characterised by measuring its transconductance and relative first and second order derivative profiles as a function of the gate voltage, to identify optimum bias point for linearity (Fig. 1). A set of load-pull measurements was made in cooperation with Politecnico di Torino, to validate optimum bias-point selection and characterise the device's non-linear behaviour. In particular, in order to cover the whole Smith Chart, the measurements were performed using an active tunable load (Pisani et al., (4)). Modelling activity has been carried out both in-house and in co-operation with the Universita' di Bologna-DEIS (complete model validation is still ongoing). MMIC power amplifier design approach has carefully considered circuit solutions, mainly for the matching networks, with lower sensitivity to electrical and geometrical parameter variations. Moreover, a balanced configuration based on Lange couplers was adopted, in order to overcome the poor input and output reflection performance of the single branch amplifier, obtaining very good return loss at any bias condition (fig. 3, 4), together with a lower sensitivity to manufacturing process dispersion. The effect of this design methodology resulted in very high yield as can be seen looking at statistical on-wafer measured data for the PA18-23 design (Fig. 2-4, more than 200 samples from 4 different wafers).

CONCLUSION

A complete development procedure set up to develop highly linear MMIC power amplifiers has been presented. Following this procedure a family of new MMIC power amplifiers for a 128-QAM radio has been designed. Experimental data of such MMIC amplifiers have also demonstrated the validity of the presented approach.

REFERENCES

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TABLES AND FIGURES

Freq. [GHz]	$\|G_{Load}\|$	Ð G_{Load} (°)	C/I3 [dBc] @ 18 dBm
13	0.46	120	44
15	0.44	125	44
18	0.58	130	46

Tab. 1

Freq. [GHz]	$\|G_{Load}\|$	Ð G_{Load} (°)	PAE
13	0.50	119	56%
15	0.56	114	52%
18	0.59	129	51%

Tab. 2

Device Name	PA13-15	PA18-23	PA26-31
Freq. band [GHz]	13-15	18.5-24	24-31.5
Percentage band	19%	26%	26%
Linear gain [dB]	18	14	10
Input RL [dB]	19	19	16
Output RL [dB]	19	20	18
P_{1dB} [dBm]	28	28	28
IP_3 [dBm]	N.A.	36.5	N.A.
$P_{D.C.}$ [W]	2.5	2.5	2.5

Tab. 3

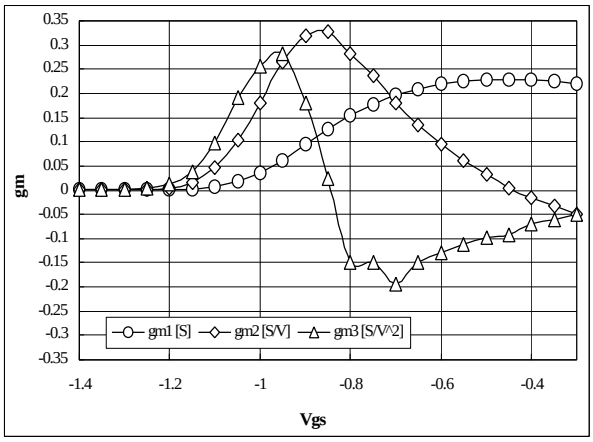

Fig. 1

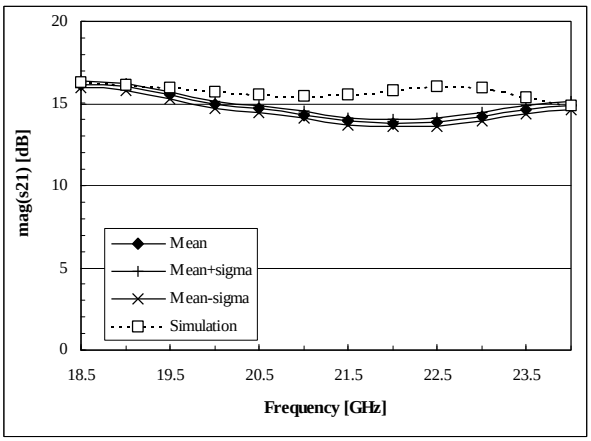

Fig. 2

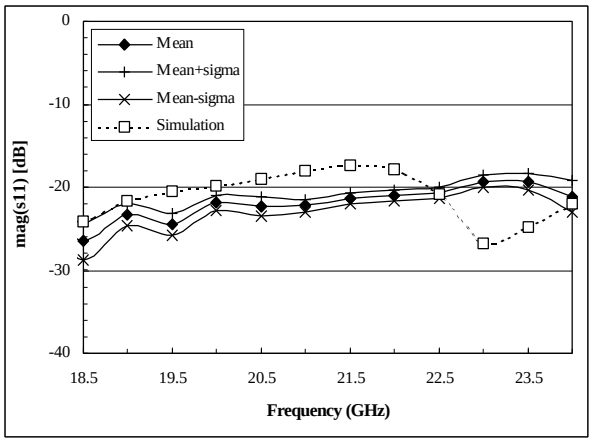

Fig. 3

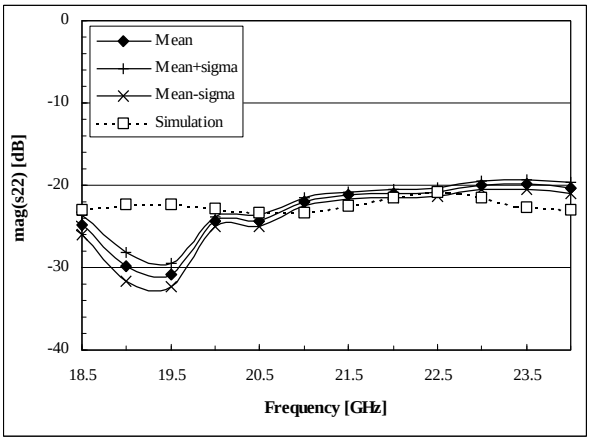

Fig. 4

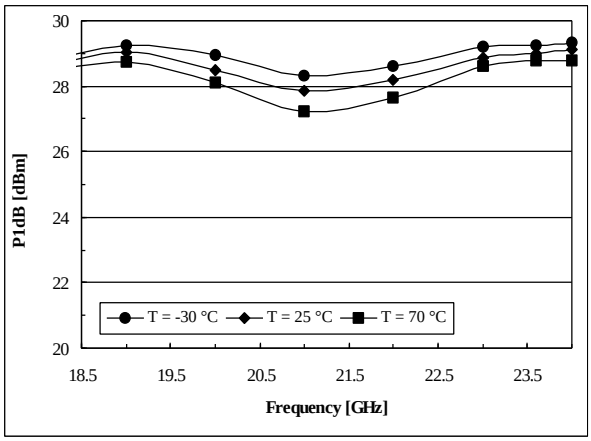

Fig. 5

CAPTIONS

Tab. 1 – Measured C/I3 optimum load values @ 18 dBm for the selected active device at different frequencies.
Tab. 2 – Measured PAE optimum load values @ 3 dB gain compression for the selected active device at different frequencies.
Tab. 3 – Main measured data for the developed MMIC (as currently available).

Fig. 1 – Measured $g_{m1}=g_m$; $g_{m2}=1/2\ g'_m$; $g_{m3}=1/6\ g''_m$ for the selected active device.
Fig. 2 – Measured PA18-23 linear gain compared with simulation.
Fig. 3 – Measured PA18-23 input Return Loss compared with simulation.
Fig. 4 – Measured PA18-23 output Return Loss.compared with simulation.
Fig. 5 – Measured PA18-23 1 dB compression point at different temperatures.